

MICROPROCESSORS AND MICROSYSTEMS

Index to Volume 12 Numbers 1-10, pages 1-600 (1988)

Subject index

Key: (AN) = application note; (DN) = design note; (PN) = product news; (TI) = teach-in

Addressing mechanism	67	Fast Fourier transform	76, 206, 471	Multiprocessing	211
Application specific ICs	245, 260	Fault tolerance	264	— bus arbitration (DN)	147
Array logic (PN)	107	Fieldbus	555	— on Nubus	147
Bus arbitration	211, 403	'Flash' EPROMs (PN)	412	— on STEBus	130
Cache memory		Floating-point operations	13, 299	— on VMEbus	513
— coherence on Nubus	147	Floating-point processors (TI)	13	Multitasking	397, 519
— consistency scheme for VMEbus	513	Formal methods	539, 547		
— mapping parameters	197	Futurebus	48, 159		
— on-chip cache design	563	GaAs devices	172, 277	NS32000	67
— page associative caches on Futurebus	159	Gate arrays (PN)	172, 245, 323	Nubus	147
— technology impact	277	Graphics coprocessors	271	Object-oriented programming	433
CAD tools		Graphics software	271	Operating systems	
— microprogram design	463	Graphics windows	397	— OS/2 (PN)	53
— semicustom design	245, 363	HD64180 microcomputer	527	— VRTX (PN)	107
Computer integrated manufacturing	24	High-level languages	153, 331, 433	Optical sensors	527
Coprocessors	271, 345	Image processing		P1396 communications bus	139
Correlation (AN)	214	— object recognition	527	Parallel architectures	397
Crossdevelopment	443	— hardware for Hough transform	490	Parallel C (PN)	354
C++	433	Industrial control	373, 383	PASCAL	331
Data buses		Industrial networking	555	Pneumatic drives	373
— Arinc 429	429	Interfacing		Programmable logic devices	164, 245
— Bitbus	3	— E ² PROMs (AN)	40		
— Ethernet	3	— TMS320-transputers	490	Realtime control (DN)	341
— Fieldbus	555	In-circuit emulator (PN)	224	Realtime systems	391, 519
— Mil-Std-1553B	3	Local area networks		Reliability	309
Debugging	33, 331	— Fieldbus	555	RISCs	
Digital correlators (AN)	214	— LAN node	383	— a review	179
Digital filters	299	M68000		— addressing mechanisms	67
Digital signal processing	76, 206, 299, 471, 485	— addressing mechanisms	67	— GaAs devices	277
Distributed software	33	Machine vision	24	— LISP oriented RISC architectures	187
Distributed systems	519	Manufacturing automation		— Mil-Std-1750A microprocessor (PN)	353
DMA controller	125	protocol (MAP)	48, 555	— MIPS architecture	277
DSP56000	299	MC68452 bus arbitration module (DN)	211	— on-chip caches	197
Dual-bank memory	206	Medical instrumentation		— R2000 (PN)	353
Dual-port memory	585	— ECC analysis	92	— 80960 (PN)	412
E ² PROMs (AN)	40	Memory management (AN)	345	— 88000 (PN)	352
Echo canceller		Memory mapping (AN)	286	Safety-critical applications	264, 539
— implementing the TMS32020	485	Messaging kernels	454	Semicustom design	245, 323, 363
Electrical interference	309	Microcontrollers	341, 532	Silicon compilers	245
Electromagnetic susceptibility	317	Microprocessor architectures		Silicon fabrication	245
Emulation	497	— Micro/370 microprocessor	419	Simulation	
Expert systems		— 68000 series	419	— 8-bit microprocessors	443
— design automation	83	Microprograms	463	— cache design	197, 277
		Microsequencers (AN)	101	— semicustom design	245, 363
		Mil-Std-1553B data bus	3	SMALLTALK 80	433
		MIPS architecture	277	Software specification	391, 539
		Modems	485, 532	Software verification	547
		Multibus I (AN)	403	Standard cells	245
		Multibus II	48	STEBus	48, 97, 130, 135
		Multipliers (AN)	471		

Telecommunications	485, 532	
Test	245, 317, 573	
TMS320 series	490	
TMS32010	206	
TMS32020	485	
TMS320C25	76, 497, 505	
TMS9900 (AN)	286	
TMS9995 (AN)	286	
Transputers	107, 354, 490	
TRON		
— addressing mechanisms	67	
— H32/200 microprocessor (PN)	411	
— microcontroller (PN)	225	
Viper microprocessor	171, 264, 539	
VLSI		
— on-chip cache	563	
— test	573	
VMEbus	48, 513	
VMEbus		
— control using PLDs (AN)	164	
— CPU architecture	153	
— fast DMA controller	125	
— to STE intercrate link	135	
Z80	40, 286, 585	
8-bit microprocessors	286, 443	
8085	463	
8086	40, 331	
8088	40	
8096	341	
32532 VME boards (PN)	225	
68000	206, 211, 419, 454, 519, 585	
68010	419	
68020	345, 419	
68030 board products (PN)	52	
80286 series peripherals (AN)	403	
80376, 'customized' 80386 (PN)	412	
80386 (AN)	403	
80960 RISC microprocessor (PN)	412	
82786 graphics coprocessor	271	
88000 RISC microprocessor (PN)	352	
Burton, P	Designing microprocessor-based equipment for immunity from electrical interference	309
Cancelo, G I	See Catalfo, J M	383
Catalfo, J M	LAN node for industrial environments	383
Chance, J	Verification of DSP simulation by comparison with the hardware	497
Chia, W H	See Furht, B	187
Chow, P	Impact of mapping parameters on the performance of small cache memories	197
Colley, M J	Parallel-architecture windowing display	397
Cottrell, R A	See Hicks, P J	245
Davies, A C	Introduction to formal methods of software design	547
Dickman, G	See Sridharan, S	299
Dixon, P	Page associative caches on Futurebus	159
Dunlop, G	See Armitage, G	555
Eldon, J	Applications of the digital correlator (AN)	214
Eswaran, C	See Natarajan, K S	532
Eswaran, C	See Umamaheswari, G	206
Frailey, D	See Tyson, T J	286
Froome, P	The role of mathematically formal methods in the development and assessment of safety-critical systems	539
Furht, B	Multiple register window file for LISP-oriented RISC architectures	187
Gallia, J	See Tyson, T J	286
Gandhi, S	Graphics software and hardware design with the 82786	271
Geigel, T and Chow, P		197
Halbert, M P	Selfchecking computer module based on the Viper microprocessor	264
Hicks, P J	Overview of semicustom IC design	245
Horne, E	TMS32020 implementation of an adaptive recursive echo canceller	485
Huber, F	See Bemmerl, T	331
Hughes, L	Design and implementation of a multicast messaging kernel	454
Hutchison, D	See Armitage, B	555
Inett, G	Multiprocessing and the STEbus	130
Intel	Interfacing the 80386 to Multibus I (AN)	403
Jhunjhunwala, A	See Umamaheswari, G	206
Kabakibo, A	Simulation study of the impact of technology on cache memory performance	277
Kamdar, J P	Commercial considerations for designing with ASICs (U)	260
Karwoski, R J	Four-cycle butterfly arithmetic architecture (AN)	471
Kingswood, N and Milford, D		363
Lai, Y N	See Furht, B	187
Laws, G	Multiprocessing on the Nubus using cache inhibited pages	147
Lazzerini, B	Event-driven debugging for distributed software	33
Masud, M	See Sait, S M	463
McCrosky, C	On the design of on-chip instruction caches	563
Milford, D	CAD tools for semicustom IC design	363
Milutinovic, A	See Kabakibo, A	277
Milutinovic, V	See Chow, P	197
Monahan, B	See Froome, P	539
Motorola	32-bit computer design using the 68020, 68881 and 68851	345
Natarajan, K S	Design of a CCITT V.22 modem (DN)	532
Nelson, G A	P1396: a proposed standard communications bus	139
Ng, K W	Low-cost distributed realtime multitasking system	519
Norris, M T	See Orr, R A	391
Ogden, D	See Tyson, T J	391
Orr, R A	Systematic method for realtime system design	391
Palmer, C	VMS serial bus as an intercrate link from VME to STE	135
Prete, C A	See Lazzerini, B	33
Pridmore, J	See Chow, P	197
Pu, J	Motion control of pneumatic drives	373
Rouch, C D V	And Orr, R A	391
Russell, R A	Optical sensory work surface for a robot manipulator system	527
Sait, S M	CAD tool for the automatic generation of microprograms	463
Sandler, M	Interfacing the transputer to the TMS320 in an image processing environment	490
Seeq Technology	E ² PROM interfacing (AN)	40
Soleit, E A	See Horne, E	485
Sridharan, S	Block floating-point implementation of digital filters using the DSP56000	299
Stampfl, R	See Bemmerl, T	331
Tabak, D	RISC systems	179
Texas Instruments	TMS320C25 digital signal processor (AN)	505
Thurlow, M	Susceptibility characterization of microprocessor and LSI technology	317
Tinker, R	See Orr, R A	391
Tredennick, N	Experiences in commercial VLSI microprocessor design	419
Tyson, T J	Using the 54/74LS610-13 memory mapping units (AN)	286
Umamaheswari, G	Signal processing implementation with a dual-bank memory	206
Van de Goor, A J	See Bril, R J	513
Van der Wateren, F	Fast DMA controller for the VMEbus	125
ven der Buhu, B	See McCrosky, C	563
Weston, R H	See Azar, I	24
Weston, R H	See Pu, J	373
Wilkins, B R	Testing methodology: implications for the circuit designer	573
Winder, R	Modelling 8-bit microprocessors for a general-purpose simulator	443
Wyland, D	Dual-port RAMs simplify processor communication	585
Yaagoub, A Y	See Sait, S M	463
York, T	Gate array architectures	323
York, T A	See Hicks, P J	245
Yu, S	See Armitage, B	555

Author index

Key: (AN) = application note; (DN) = design note; (TI) = teach-in; (U) = update

Aboalsamh, H A	See Furht, B	187
Advanced Micro Devices	IEEE floating-point format (TI)	13
Advanced Micro Devices	Simplified VMEbus control using programmable logic devices (AN)	164
Anderson, B	Object-oriented programming	433
Armitage, B	Fieldbus: an emerging communications standard	555
Azar, I	On vision architecture for computer integrated manufacturing	24
Barany, T E	Fast evaluation of integer roots in microcontroller systems (DN)	341
Bemmerl, T	Features, design and implementation of high-level language debuggers	331
Boukerrou, R	Arbitration unit for multiprocessor systems using a shared bus (DN)	211
Bracknell, D	Introduction to the Mil-Std-153B serial multiplex data bus	3
Bril, R J	Software transparent cache consistency scheme for a VMEbus-based system	513
Burnley, P	CPU architecture for realtime VME systems	153

Title index

32-bit computer design using the 68020, 68881 and 68851	345
Applications of the digital correlator (AN)	214
Arbitration unit for multiprocessor systems using a shared bus (DN)	211
Block floating-point implementation of digital filters using the DSP56000	299
CAD tool for the automatic generation of microprograms	463
CAD tools for semicustom IC design	363
Commercial considerations for designing with ASICs (U)	260
CPU architecture for realtime VME systems	153
Design and implementation of a multicast messaging kernel	454
Design of a CCITT V.22 modem (DN)	532

Designing microprocessor-based equipment for immunity from electrical interference	309	Introduction to formal methods of software design	547	Signal processing implementation with a dual-bank memory	206
Dual-port RAMs simplify processor communication	585	Introduction to the Mil-Std-1553B serial multiplex data bus	3	Simplified VMEbus control using programmable logic devices (AN)	164
E ² PROM interfacing (AN)	40	LAN node for industrial environments	383	Simulation study of the impact of technology on cache memory performance	227
Event-driven debugging for distributed software	33	Low-cost distributed realtime multitasking system	519	Software transparent cache consistency scheme for a VMEbus-based system	513
Experiences in commercial VLSI microprocessor design	419	Modelling 8-bit microprocessors for a general-purpose simulator	443	Susceptibility characterization of microprocessor and LSI technology	317
Fast DMA controller for the VMEbus	125	Motion control of pneumatic drives	373	Systematic method for realtime system design	391
Fast evaluation of integer roots in microcontroller systems (DN)	341	Multiple register window file for LISP-oriented RISC architectures	187	Testing methodology: implications for the circuit designer	573
Features, design and implementation of high-level language debuggers	331	Multiprocessing and the STEbus	130	The role of mathematically formal methods in the development and assessment of safety-critical systems	539
Fieldbus: an emerging communications standard	555	Multiprocessing on the Nubus using cache inhibited pages	147	TMS32020 implementation of an adaptive recursive echo canceller	485
Four-cycle butterfly arithmetic architecture (AN)	471	Object-oriented programming	433	TMS320C25 digital signal processor (AN)	505
Gate array architectures	323	On the design of on-chip instruction caches	563	Using the 54/74LS610-13 memory mapping units (AN)	286
Graphics software and hardware design with the 82786	271	Optical sensory work surface for a robot manipulator system	527	Verification of DSP simulation by comparison with the hardware	497
IEEE floating-point format (TI)	13	Overview of semicustom IC design	245	VME serial bus as an intercrate link from VME to STE	135
Impact of mapping parameters on the performance of small cache memories	197	P1396: a proposed standard communications bus	139		
Interfacing the 80386 to Multibus I (AN)	403	Page associative caches on Futurebus	159		
Interfacing the transputer to the TMS320 in an image processing environment	490	Parallel-architecture windowing display	397		
		RISC systems	179		
		Selfchecking computer module based on the Viper microprocessor	264		